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GreenChip III TEA1750: integrated PFC and flyback controller

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Document information

Info	Content
Keywords	GreenChip III, TEA1750, PFC, flyback, high efficiency, adaptor, notebook, LCD TV, PC Power.
Abstract	The TEA1750 is a member of the new generation of PFC and flyback controller combination ICs, used for efficient switched mode power supplies. It has a high level of integration which allows the design of a cost effective power supply with a very low number of external components. The TEA1750 is fabricated in a Silicon On Insulator (SOI) process. The NXP SOI process makes a wide voltage range possible.

Revision history

Rev	Date	Description
01	20090210	First release

Contact information

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1. Introduction

The TEA1750 is a combination controller with a PFC and flyback controller integrated in to an SO-16 package. Both controllers operate in QR / DCM mode with valley detection. The switching is independent for each controller.

The PFC output power is on-time controlled for simplicity. It is not necessary to sense the phase of the mains voltage. The flyback output power is Current mode controlled for good suppression of input voltage ripple.

The communication circuitry between both controllers is integrated and no adjustment is needed.

The voltage and current levels mentioned in this application note are typical values. A detailed description of the pin level spreading can be found in the *TEA1750 data sheet*.

1.1 Scope

This application note describes the functionality and the control functions of the TEA1750 and the adjustments needed within the power converter application.

For the large signal parts of the PFC and flyback power stages, the design and data for the coil and transformer are dealt with in a separate application note.

1.2 The TEA1750 GreenChip III controller

The features of the GreenChip III allow the power supply engineer to design a reliable and cost effective and efficient switched mode power supply with the minimum number of external components.

1.2.1 Key features

- PFC and flyback controller integrated in one SO-16 package
- Switching frequency of PFC and flyback are independent of each other
- No external hardware required for communication between the two controllers
- High level of integration, resulting in a very low external component count
- Mains voltage enable and brown-out protection integrated
- Fast latch reset function implemented

1.2.2 System features

- Safe Restart mode for system fault conditions
- High voltage start-up current source (5.4 mA)
- Reduction of HV current source (1 mA) in Safe Restart mode
- Wide V_{CC} range (38 V)
- MOSFET driver voltage limited
- Easy controlled start-up behaviour and V_{CC} circuit
- Small PFC bulk elcap possible (82 uF @ 120 W)
- General purpose input for latched protection

- Internal IC overtemperature protection
- Two high voltage spacers between the HV pin and the next active pin
- Open pin protection on the VINSENSE, VOSENSE, PFCAUX, FBCTRL and FBAUX pins

1.2.3 PFC features

- Quasi-resonant / DCM operation with valley switching
- Frequency limitation (125 kHz) to reduce switching losses and EMI
- T_{on} controlled
- Mains input voltage compensation for control loop for good transient response
- OverCurrent Protection (OCP)
- Burst mode at low and no-load (controlled by the flyback controller)
- Soft start and soft stop
- Open / short detection for PFC feedback loop, no external OVP circuit necessary

1.2.4 Flyback features

- Quasi-resonant / DCM operation with valley switching
- Frequency limitation (12 5kHz) to reduce switching losses and EMI
- Current mode controlled
- Overcurrent protection
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels without audible noise
- Soft start
- Accurate OverVoltage Protection (OVP) through auxiliary winding
- Time-out protection for output overloads and open flyback feedback loop.

1.3 Application schematic

Figure 1 shows the complete functional schematic of the TEA1750 application.

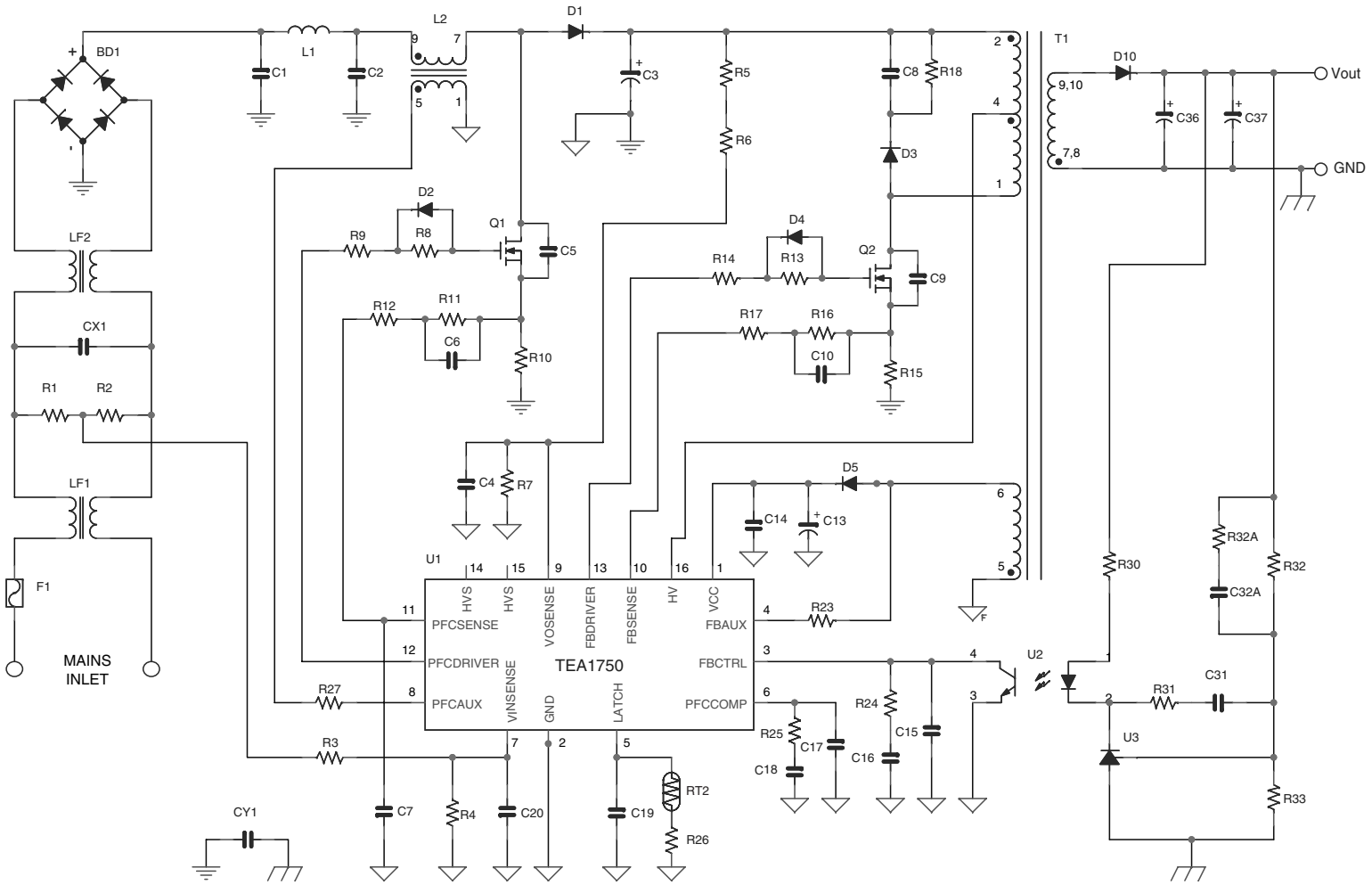

Fig 1. Application schematic

2. Pin description

Table 1. Pin description

Pin	Name	Functional description
1	VCC	Supply voltage: $V_{startup}$ = 22 V, $V_{th(UVLO)}$ = 15 V. At mains switch-on, the capacitor connected to this pin is charged to $V_{startup}$ by the internal HV current source. When the pin voltage is lower than 0.65 V, the charge current is limited to 1 mA, this to prevent overheating of the IC if the V_{CC} pin is short circuited. When the pin voltage is between 0.65 V and $V_{th(UVLO)}$, the charge current is 5.4 mA to enable a fast start-up. Between $V_{th(UVLO)}$ and $V_{startup}$, the charge current is again limited to 1 mA, this to reduce the safe restart duty cycle and as a result the input power during fault conditions. At the moment $V_{startup}$ is reached the current source is pinched-off, and V_{CC} is regulated to $V_{startup}$ till the flyback starts. See Section 3.2 for a complete description of the start-up sequence.
2	GND	Ground connection.
3	FBCTRL	Control input for flyback for direct connection of the opto-coupler. At a control voltage of 2 V the flyback will deliver maximum power. At a control voltage of 1.5 V the flyback will enter the Frequency Reduction mode and the PFC will be set into Burst mode. At 1.4 V the flyback will stop switching. Internal there is a 30 μA current source connected to the pin, which is controlled by the internal logic. This current source can be used to implement a time-out function to detect an open control loop or a short circuit of the output voltage. The time-out function can be disabled with a resistor of 100 kΩ between this pin and ground.
4	FBAUX	Input from auxiliary winding for transformer demagnetization detection and overvoltage protection (OVP) of the flyback. The combination of the demagnetization detection at the FBAUX pin and the valley detection at the HV pin are determining the switch-on moment of the flyback in the valley. A flyback OVP is detected at a current > 300 μA into the FBAUX pin. Internal filtering is present to prevent false detection of an OVP at mains transients or an ESD event.
5	LATCH	General purpose latched protection input. When $V_{startup}$ (pin 1) is reached, this pin is charged to a voltage of 1.35 V first before the PFC is enabled. To trigger the latched protection the pin has to be pulled down to below 1.25 V. An internal 80 μA current source is connected to the pin, which is controlled by the internal logic. Because of this current source, a NTC resistor for temperature protection can be directly connected to this pin.
6	PFCCOMP	Frequency compensation pin for the PFC control loop.

Table 1. Pin description

Pin	Name	Functional description
7	VINSENSE	Sense input for mains voltage. This pin has 4 functions: • mains enable level: $V_{start(VINSENSE)}$ = 1.15 V; • mains stop level (brown-out): $V_{stop(VINSENSE)}$ = 0.9 V; • mains voltage compensation for the PFC control-loop gain bandwidth; fast latch reset: V_{flr} = 0.75 V. • The mains-enable and mains-stop level will enable and disable the PFC. Enabling and disabling the flyback is controlled through a comparator at the VOSENSE pin. The voltage at the VINSENSE pin must be an averaged DC value, representing the AC line voltage. The pin is not used for sensing the phase of the mains voltage.
8	PFCAUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control the PFC switching. The auxiliary winding needs to be connected by a 5 kΩ series resistor to prevent damage of the input due to lightning surges.
9	VOSENSE	Sense input for output voltage of the PFC. VOSENSE pin, short detection: $V_{th(ol)(VOSENSE)}$ = 0.4 V Regulation of PFC output-voltage: $V_{reg(VOSENSE)}$ = 2.5 V PFC soft-OVP (switching cycle by switching cycle): $V_{ovp(VOSENSE)}$ = 2.63 V PFC burst window lower voltage: $V_{burst(L)}$ = 1.92 V PFC burst window upper voltage: $V_{burst(H)}$ = 2.24 V Flyback start voltage: $V_{start(fb)}$ = 1.72 V Flyback stop voltage: $V_{stop(fb)}$ = 1.6 V
10	FBSENSE	Current sense input for flyback. At this pin, the voltage across the flyback current sense resistor is measured. The setting of the sense level is determined by the FBCTRL voltage, using the equation: $V_{FBSENSE} = 0.75 \times V_{FBCTRL} - 1$ V. The maximum setting level for $V_{FBSENSE}$ = 0.5 V. Internal there is a 60 μA current source connected to the pin, which is controlled by the internal logic. The current source is used to implement a soft start function for the flyback and to enable the flyback. The flyback will only start when the internal current source is able to charge the soft start capacitor to a voltage of more than 0.5 V, therefore a minimum soft start resistor of 12 kΩ is required to guarantee the enabling of the flyback.
11	PFCSENSE	Overcurrent protection input for PFC. This input is used to limit the maximum peak current in the PFC core. The PFCSENSE is a cycle by cycle protection, at 0.5 V the PFC MOSFET is switched off. There is an internal 60 μA current-source connected to the pin, which is controlled by the internal logic. This current source is used to implement a soft start and soft stop function for the PFC, this to prevent audible noise in PFC Burst mode. This pin is also used for enabling of the PFC. The PFC will only start when the internal current source is able to charge the soft start capacitor to a voltage of more than 0.5 V, therefore a minimum soft start resistor of 12 kΩ is required to guarantee the enabling of the PFC.
12	PFCDRIVER	Gate driver output for PFC MOSFET.
13	FBDRIVER	Gate driver output for flyback MOSFET.

Table 1. Pin description

Pin	Name	Functional description
14	HVS	High voltage safety spacer, not connected
15	HVS	High voltage safety spacer, not connected
16	HV	High voltage input for internal start-up current source (output at pin 1), and valley sensing of the flyback. The combination of the demagnetization detection at the FBAUX pin and the valley detection at the HV pin are determining the switch-on moment of the flyback in the valley.

3. System description and calculation

3.1 PFC and flyback start conditions

In Figure 2 and Figure 3, the conditions for enabling of the PFC and flyback are given. In case of start-up problems these condition can be checked to find the cause of the problem. Some of the conditions are dynamic signals (see Figure 4) and should be checked with an oscilloscope.

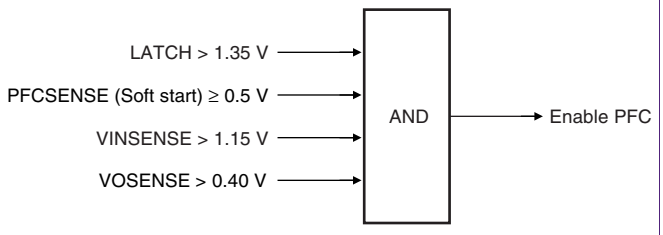

Fig 2. PFC start condition

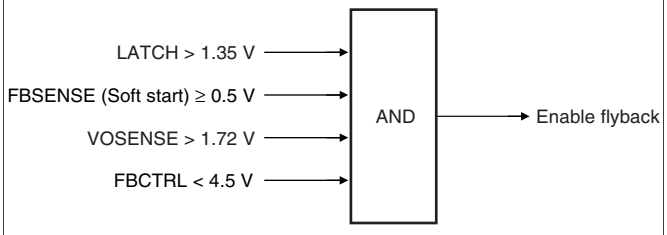

Fig 3. Flyback start conditions

3.2 Start-up sequence at a low mains voltage

At switch on with a low mains voltage, the TEA1750 power supply has the following start-up sequence (see also Figure 4):

1. The HV current source is set to 1 mA and the V_{CC} elcap is charged to 0.65 V; this to detect a possible short circuit at pin V_{CC}.
2. At V_{CC} = 0.65 V, the HV current source is set to 5.4 mA and the V_{CC} elcap is fast charged to $V_{TH(UVLO)}$.
3. At V_{CC} = $V_{TH(UVLO)}$, the HV current source is set to 1 mA again and the V_{CC} elcap is charged further to Vstartup.
4. At $V_{startup}$, the HV current source is switched off and the 80 mA LATCH pin current source is switched on to charge the LATCH pin capacitor. At the same time the PFCSENSE and FBSENSE soft start current sources are switched on.
5. When the LATCH pin is charged up to 1.35 V the HV current source is switched on again and the V_{CC} elcap is charged and regulated to $V_{startup}$.
6. When the VINSENSE pin has reached a level of 1.15 V, the PFC can start switching, but only if the PFCSENSE pin is charged up to 0.5 V and the LATCH pin is charged to 1.35 V. Also the VOSENSE pin must be >0.4 V. The VOSENSE pin will always be >0.4 V at 90 V (AC), unless there is a short circuit.

7. When the VOSENSE pin detects 1.72 V (equal to approximately 265 V (DC) at the boost elcap), the HV current source is switched off, the FBCTRL time-out current source is switched on, and the flyback is started. The flyback is only started when the FBSENSE pin is charged to 0.5 V, and the FBCTRL pin is below 4.5 V. Normally the FBCTRL pin will be below 4.5 V at the first flyback switching cycle, unless the FBCTRL pin is open.
8. When the flyback has reached its nominal output voltage, then the V_{CC} supply of the IC is taken over through the auxiliary winding. If, for any reason, the flyback feedback loop signal is missing, then the time-out protection at the FBCTRL will be triggered and both converters the PFC and the flyback will be switched off. V_{CC} will drop to $V_{TH(UVLO)}$ and the IC will continue with step 3 of the start-up cycle as described in Section 3.2. This is the safe restart cycle.

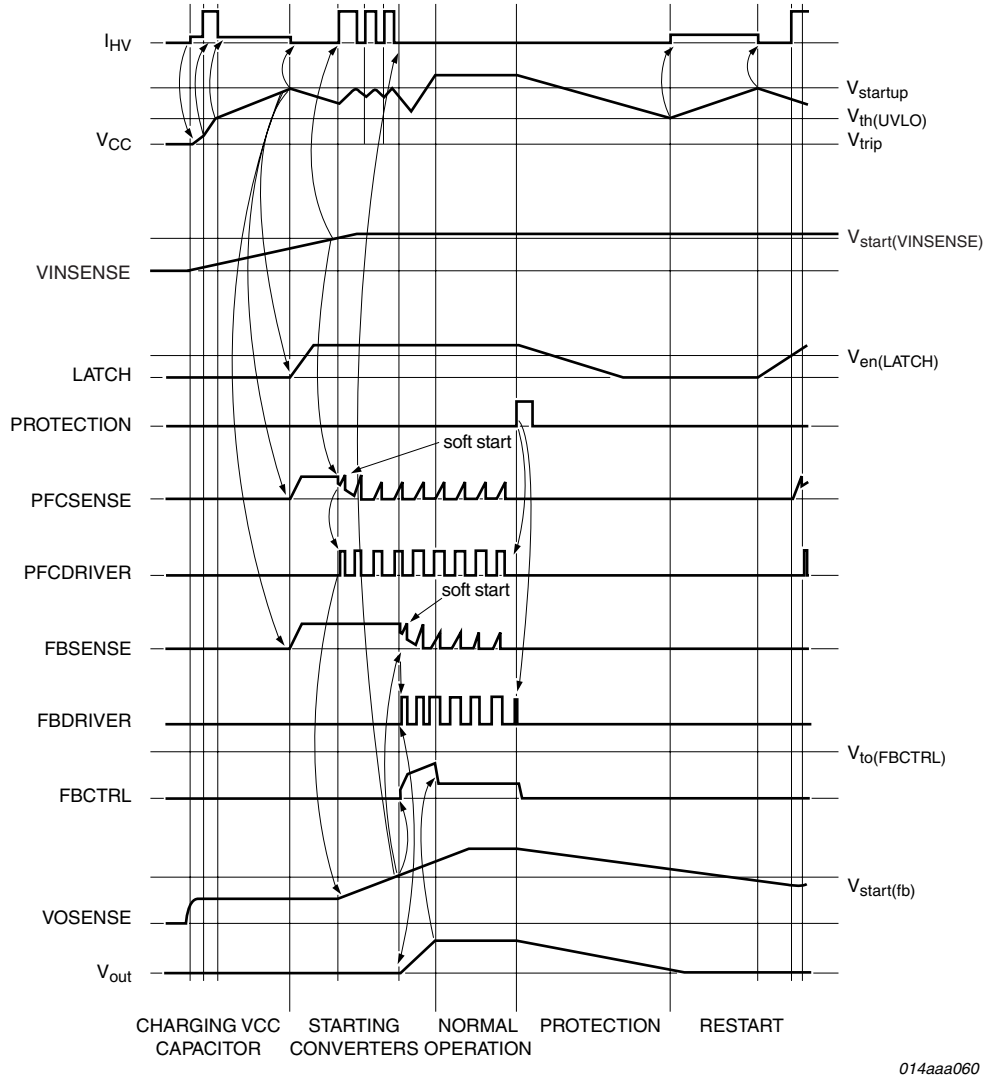

Fig 4. Start-up sequence at a low mains voltage

3.3 Start-up sequence at high mains

For the internal IC logic, the start-up sequence at high mains is equal to the start-up sequence at low mains. In the application however, there are some differences.

At switch-on with a high mains voltage, the rectified mains is causing a voltage at the VOSENSE pin which is instantaneously above the $V_{start(FB)}$ level of 1.72 V, therefore steps 6 and 7 as described in Section 3.2 will be merged. The PFC and flyback will start at the same time, but only if the VINSENSE pin has reached 1.15 V, the LATCH pin is charged to 1.35 V and both soft start capacitors at the PFCSENSE pin and the FBSENSE pin are charged to 0.5 V. The charge time of the soft start capacitors can be chosen by their values independently for the PFC and the flyback. This way it can be realized that the PFC starts before the flyback.

3.4 V_{CC} cycle at safe restart protections

In Safe Restart mode the controller will go through the steps 3 to 8 as described in Section 3.2 and Section 3.3.

3.5 Mains voltage sensing and brownout

The mains input voltage is measured at the VINSENSE pin. When the VINSENSE pin has reached the $V_{start(VINSENSE)}$ level of 1.15 V, the PFC can start switching, but only if the other start conditions shown in Section 3.1 are also met. As soon as the voltage at the VINSENSE pin drops below the $V_{stop(VINSENSE)}$ level of 0.89 V, the PFC will stop switching. The flyback will continue switching until the level at the VOSENSE pin has dropped below the $V_{stop(fb)}$ level of 1.6 V.

The voltage at the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimal with a time constant of approximately 150 ms at the VINSENSE pin. The long time constant at the VINSENSE pin would prevent a fast restart of the PFC after a mains drop-out, therefore the voltage at the VINSENSE pin is clamped to a level of 100 mV below the $V_{start(VINSENSE)}$ level, this to guarantee a fast PFC restart after recovery of the mains input voltage.

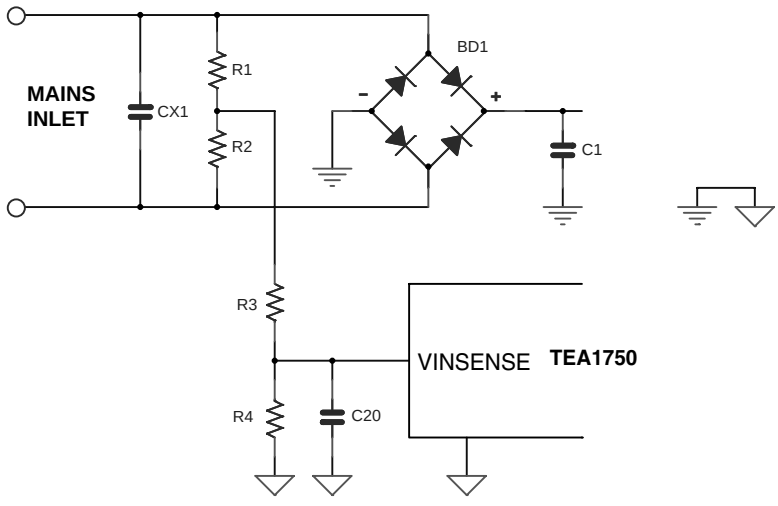

Fig 5. VINSENSE circuitry

3.5.1 Discharge of mains input capacitor

For safety, according to Ref. 1, the X-capacitors in the EMC input filtering must be discharged with a time constant $\tau < 1$ s.

The resistor to discharge the X-cap in the input filtering, is determined by the replacement value of R1+ R2.

In a typical 90 W adapter application with Cx1 = 220 nF, the replacement value of R1 + R2 must be smaller than or equal to the following:

$$R_V \leq \frac{\tau}{C} = \frac{1}{220nF} = 4.55M\Omega$$

3.5.2 Brownout voltage adjustment

The rectified AC input voltage is measured via R1 and R2. Each resistor alternately senses half the sine wave, so both resistors must have the same value.
The average voltage sensed at the connection of R1 and R2 is as follows:

$$V_{avg} = \frac{2\sqrt{2}}{\pi} \cdot V_{acrms}$$

The V (AC) brownout RMS level is calculated as follows:

$$Vac_{brownout} = \frac{\pi}{2\sqrt{2}} \cdot V_{stop(VINSENSE)} \cdot 2 \cdot \left(\frac{\frac{R1 \cdot R2}{R1 + R2} + R3}{R4} + 1 \right)$$

where: $V_{stop(VINSENSE)} = 0.89$ V

For a brownout threshold of 68 V (AC) and compliance with Ref. 1. Example values are shown in Table 2.

Table 2. VINSENSE component values

Cx1	R1	R2	R3	R4
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

A value of 3.3 μF for capacitor C20, with 47 kΩ at R4, gives the recommended time constant of ~150 ms at the VINSENSE pin.

3.6 Internal OTP

The IC has an internal temperature protection to protect the IC from overheating by overloads at the V_{CC} pin. When the junction temperature exceeds the thermal shutdown temperature, the IC will stop switching. As long as the OTP is active, the V_{CC} capacitor will not be recharged from the HV mains. The OTP circuit is supplied from the HV pin if the V_{CC} supply voltage is not sufficient. The OTP is a latched protection.

3.7 LATCH pin

The LATCH pin is a general purpose input pin, which can be used to latch both converters off. The pin sources a bias current $I_{o(LATCH)}$ of 80 μA for the direct connection of a NTC. When the voltage on this pin is pulled below 1.25 V, switching of both converters will be immediately stopped. V_{CC} will start cycling between the $V_{TH(UVLO)}$ and $V_{startup}$, without a restart. Switching off and then switching on the mains input voltage will trigger the fast latch reset circuit, and reset the latch.

At start-up, the latch pin first has to be charged above 1.35 V, before both converters are enabled. Charging of the LATCH pin starts at $V_{startup}$.

No internal filtering is present at the LATCH pin. A 10 nF capacitor must be placed between this pin and IC GROUND pin to prevent false triggering, also when the LATCH pin function is not used.

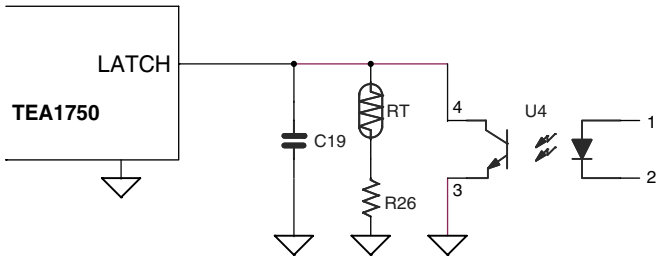

Fig 6. Usage of the LATCH pin protection

Latching on application over temperature occurs when the total resistance value of the NTC and its series resistor drops below the following:

$$R_{OTP} = \frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = \frac{1.25V}{80\mu A} = 15.6k\Omega$$

The opto-coupler triggers the latch if the driven opto transistor conducts more than 80 μA.

3.8 Fast latch reset

Switching off and then switching on the mains input voltage, can reset the latched protection. After the mains input is switched off, the voltage at the VINSENSE pin will drop below VFLR (0.75 V). This will trigger the fast latch reset circuit, but will not reset the latched protection. After the mains input is switched on, the voltage at the VINSENSE pin will rise again, and when the level has passed 0.85 V, the latch will be reset. The system will restart again when the V_{CC} pin is charged to $V_{startup}$. See step 4 of Section 3.2

4. PFC description and calculation

The PFC operates in Quasi Resonant (QR) mode or Discontinuous Conduction mode (DCM) with valley detection to reduce the MOSFET switch-on losses. The maximum switching frequency of the PFC is limited to 125 kHz to reduce the switching losses. One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz.

The PFC of the TEA1750 is designed as a boost converter with a fixed output voltage. The advantage of such a fixed boost, is that the flyback transformer can be designed to a high input voltage with limited voltage variation. This makes the design easier as the losses in the flyback transformer are smaller. Dealing with the losses in the flyback transformer can be the most challenging part of a high power flyback design.

Another advantage of the fixed output voltage PFC is the possibility to use a smaller bulk elcap value or to have a significant longer hold-up time.

In the TEA1750 system, the PFC is always active. At low mains the PFC is switched on first. The flyback is switched on after the boost elcap is charged to a level of approximately 265 V (DC). At high mains input voltage, the PFC and flyback will start at the same time, since Vac x ÷2 is already higher than 265 V (DC) when the mains is switched on.

At low output loads, the PFC is set into Burst mode. At no-load, one burst sequence can be seen every few seconds; therefore the active PFC has no significant contribution to the no-load standby power. In Burst mode the output voltage of the PFC will cycle between approximately 295 V (DC) and 345 V (DC), depending on the setting of the nominal PFC output voltage. At a high mains input voltage and low loads, the internal IC logic is also set in Burst mode. This is not noticeable because the lower level of the Burst mode window will never be reached in this case.

4.1 PFC output power and voltage control

The PFC of the TEA1750 is on-time controlled, therefore it is not necessary to measure the mains phase angle. The on-time is kept constant during the half sine wave to obtain a good power factor (PF), and compliance with class-D Mains Harmonics Reduction (MHR) according to Ref. 2.

The PFC output voltage is controlled through the VOSENSE pin. At the VOSENSE pin there is a trans-conductance error amplifier with a reference voltage of 2.5 V. The error at the VOSENSE pin is converted with 80 μA / V into a current at the PFCCOMP pin. The voltage at the PFCCOMP pin, in combination with the voltage at the VINSENSE pin, determines the PFC on-time.

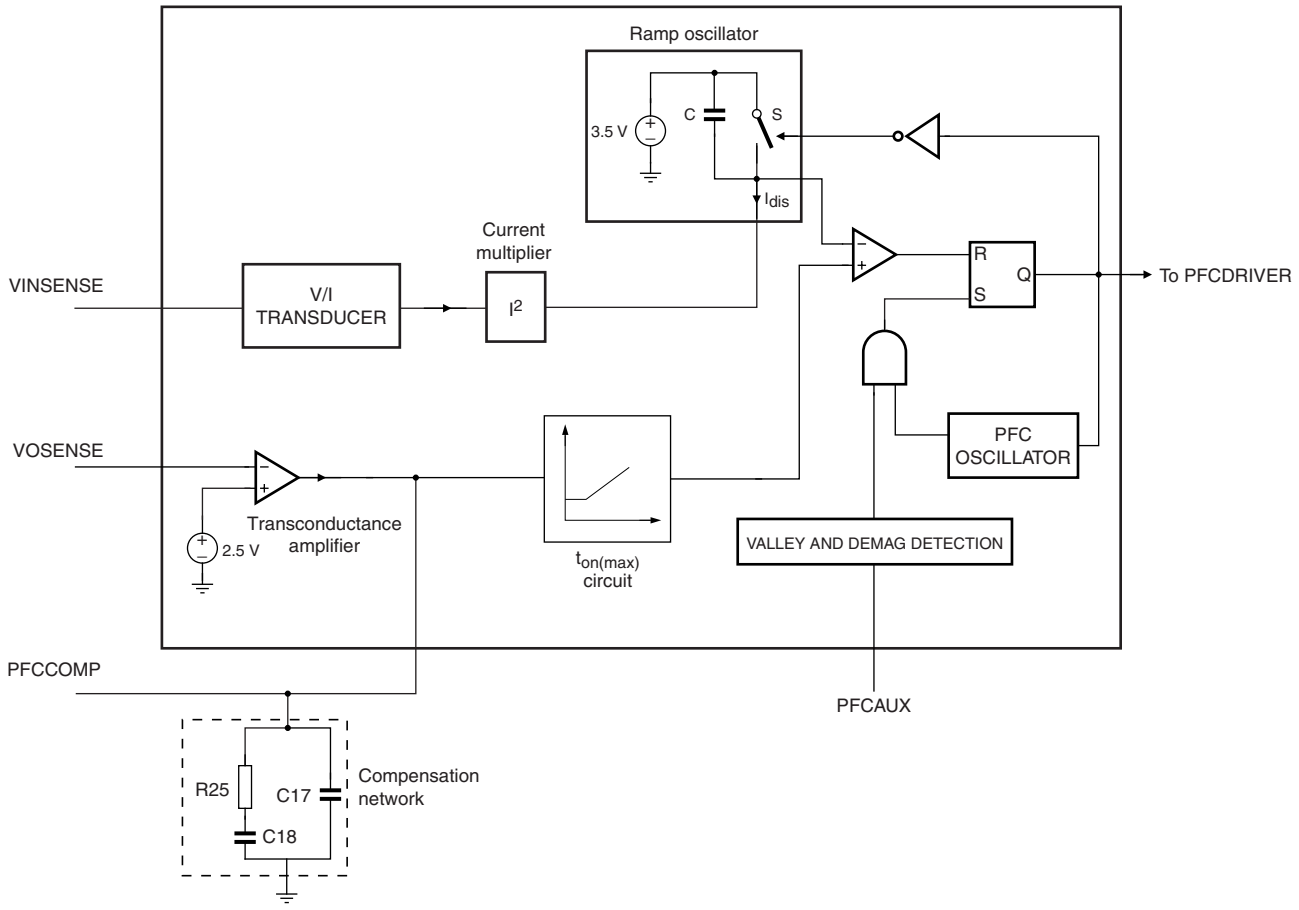

Fig 7. PFC on-time control

To stabilize the PFC control loop, a network with one resistor and two capacitors at the PFCCOMP pin is used. The mathematical equation for the transfer function of a boost converter contains the square of the mains input voltage. In a typical application this will result in a low regulation bandwidth for low mains input voltages and a high regulation bandwidth at high input voltage, while at high mains input voltages it can be difficult to meet the MHR requirements. The TEA1750 uses the mains input voltage measured through the VINSENSE pin to compensate the control loop gain as function of the mains input voltage. As a result the gain will be constant over the entire mains input voltage range.

The voltage at the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimal with a time constant of approximately 150 ms at the VINSENSE pin.

4.1.1 Setting the PFC output voltage

The PFC output voltage is set with a resistor divider between the PFC output voltage and the VOSENSE pin. In PFC Normal mode, the PFC output voltage is regulated so that the voltage on the VOSENSE pin is equal to $V_{reg(VOSENSE)}$ = 2.5 V.

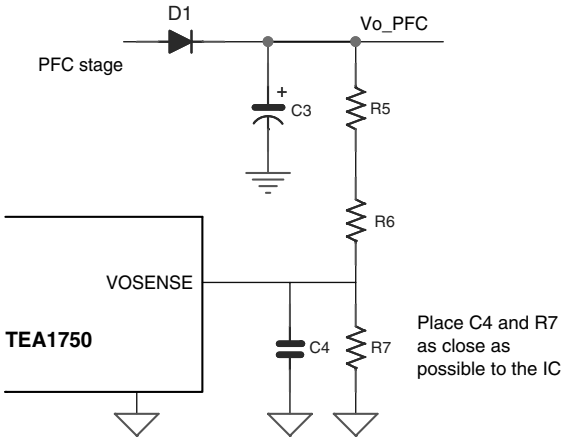

Fig 8. PFC output voltage setting

For low no-load input power two resistors of 4.7 MΩ (1%) can be used between the bulk elcap and the VOSENSE pin.

The resistor R7 (1%) between the VOSENSE pin and ground can be calculated with equation:

$$R7 = \frac{(R5 + R6) \times V_{reg(VOSENSE)}}{(Vo_{PFC} - V_{reg(VOSENSE)})}$$

Suppose the regulated PFC output voltage is 382 V, then:

$$R7 = \frac{(4.7M\Omega + 4.7M\Omega) \times 2.5V}{(382V - 2.5V)} = 62k\Omega(1\%)$$

The function of the capacitor C4 at the VOSENSE pin, is to filter noise and to prevent false triggering of the protections, due to MOSFET switching noise, mains surge events or ESD events. False triggering of the $V_{ovp(VOSENSE)}$ protection can cause audible noise and disturbance of the AC mains input current. False triggering of the $V_{th(ol)(VOSENSE)}$ protection will cause a safe restart cycle. A time constant of 500 ns to 1 ms, at the VOSENSE pin should be sufficient, which results in a value of 10 nF for capacitor C4.

It is advised to place R7 and C4 as close as possible to the IC between the VOSENSE pin and the IC ground pin.

4.2 PFC Burst mode

At low output loads and no-load the PFC operates in Burst mode. The flyback is determining the power level where the PFC goes into Burst mode. With the a correct setting of the flyback current sense resistor value, the PFC is set into Burst mode at approximately 15 % of the maximum flyback output power. See also Section 5.1. In Burst mode, the output voltage of the PFC is cycling in a window with an upper and lower voltage level. The upper and lower level is determined by the setting of the external voltage divider at the VOSENSE pin in combination with the internal levels.

During normal operation, the output voltage of the PFC is regulated so that the voltage $V_{reg(VOSENSE)}$ at the VOSENSE pin, remains at 2.5 V. When the PFC is set into Burst mode, the following sequence is used:

1. The PFC is switched off.
2. The voltage on the bulk elcap will drop until the voltage at the VOSENSE pin reaches the $V_{burst(L)}$ level of 1.92 V.
3. At the $V_{burst(L)}$ level the PFC is switched on again and the bulk elcap is charged until the voltage at the VOSENSE pin reaches the $V_{burst(H)}$ level of 2.24 V.
4. At the $V_{burst(H)}$ level the PFC is switched off again.

As long as the Burst mode is active, the PFC will continue to cycle between steps 2 and 4 in Section 4.2.

At the transition from PFC Burst mode to PFC Normal mode, the PFC is switched on again and the bulk elcap is charged until the voltage at the VOSENSE pin reaches the $V_{reg(VOSENSE)}$ level of 2.5 V.

To prevent audible noise due to starting and stopping of the PFC in Burst mode, the PFC logic is controlling a soft start at the $V_{burst(L)}$ level and a soft stop at the $V_{burst(H)}$ level.

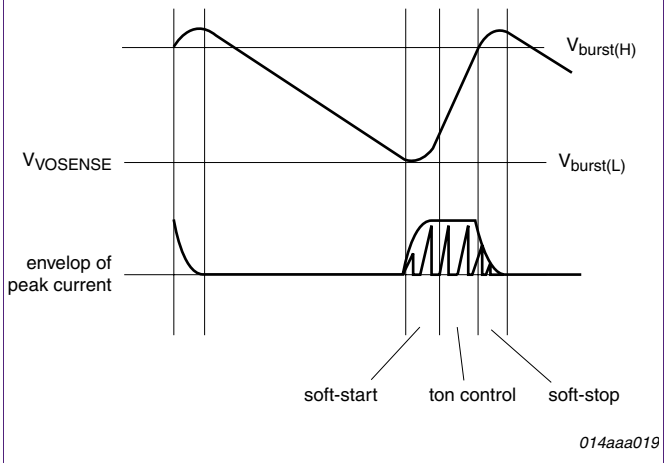

Fig 9. PFC Burst mode control

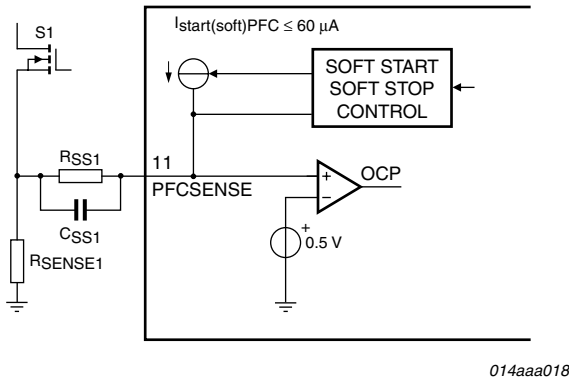

Fig 10. PFC soft start and soft stop

4.2.1 Calculation of the PFC soft start and stop components

The soft start and stop are implemented through the RC network at the PFCSENSE pin.

Rss1 must have a minimum value of 12 kΩ as specified. This to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable start-up of the PFC. See Section 3.1 for start-up description.

The total soft start or soft stop time is equal to: $t_{softstart} = 3Rss1 \cdot Css1$

It is advised to keep the soft start time of the PFC smaller than the soft start time of the flyback to ensure that the PFC starts before the flyback at initial start-up. It is also advised that the soft start time is kept within a range of 2 ms to 5 ms.

With C8 = 100 nF and R11 = 12 kW, the total soft start time will be 3.6 ms.

4.3 PFC demagnetizing and valley detection

The PFC MOSFET is switched on again after the transformer is demagnetized. The internal IC circuit connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage at the drain of the PFC MOSFET. The next stroke is started when the voltage at the drain of the PFC MOSFET is at its minimum (valley switching) in order to reduce switching losses and electromagnetic interference (EMI).

The maximum switching frequency of the PFC is limited to 125 kHz to reduce the switching losses. One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz.

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS), 50 ms after the start of the last PFCDRIVER signal.

If no valley signal is detected on the PFCAUX pin, the controller generates an internal valley signal 4 ms after demagnetization was detected.

See Figure 12 for applications with high transformer ringing frequencies (after the secondary stroke), the PFCAUX pin should be connected via a capacitor and a resistor to the auxiliary winding to prevent incorrect skipping of valleys. A diode with a parallel resistor 1 MΩ must then be placed from the PFCAUX pin to ground.

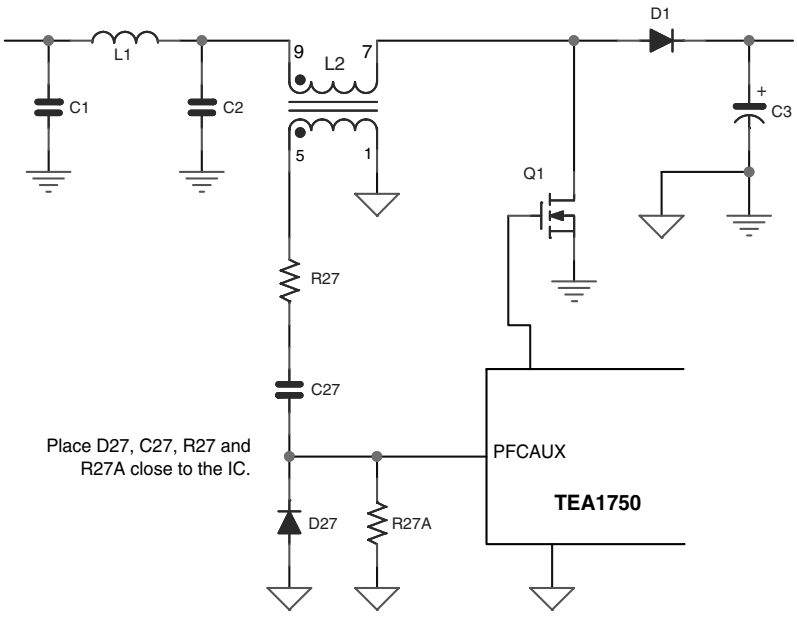

Fig 11. PFCAUX circuitry

4.3.1 Design of the PFCAUX winding and circuit

To guarantee valley detection at low ringing amplitudes, the voltage at the PFCAUX pin should be set as high as possible, taking into account its absolute maximum rating of ±25 V.

The number of turns of the PFCAUX winding can be calculated as follows:

$$N_{a\_max} = \frac{V_{PFCaux}}{V_{Lmax}} \times N_p = \frac{25V}{V_{Lmax}} \times N_p$$

Where: V_{PFCAUX} is the absolute maximum rating of the PFCAUX pin, and V_{Lmax} is the maximum voltage across the PFC primary winding. The PFC output voltage at the PFC OVP level determines the maximum voltage across the PFC primary winding and can be calculated with equation:

$$V_{Lmax} = \frac{V_{OVP(VOSENSE)}}{V_{reg(VOSENSE)}} \times Vo_{PFC} = \frac{2.63V}{2.5V} \times Vo_{PFC}$$

When a PFC coil with a higher number of auxiliary turns is used, then a resistor voltage divider can be placed between the auxiliary winding and pin PFCAUX. The total resistive value of the divider should be less than 10 kΩ to prevent delay of the valley detection by parasitic capacitance.

The polarity of the signal at the PFCAUX pin must be reversed compared to the PFC MOSFET drain signal.

To protect the PFCAUX pin against electrical overstress, for example during lighting surge events, it is advised to have a 5 kW resistor between the PFC auxiliary winding and this pin. To prevent incorrect valley switching of the PFC due to external disturbance, the resistor should be placed close to the IC.

4.4 PFC protections

4.4.1 VOSENSE Over Voltage Protection

At start-up or at the transition from PFC Burst mode to PFC Normal mode, a voltage overshoot can occur at the boost elcap. This overshoot is caused by the relative slow response of the PFC control loop. The PFC control loop response must be relatively slow to guarantee a good power factor and meet the MHR requirements. The Over Voltage Protection (OVP) at the VOSENSE pin will limit the overshoot. At the moment that the $V_{OVP(VOSENSE)}$ level of 2.63 V is detected, the PFC MOSFET is switched off immediately, regardless of the on time setting. The switching of the MOSFET remains blocked until the voltage at the VOSENSE pin drops below 2.63 V again.

The peak voltage at the boost elcap generated by the PFC due to an overshoot and limited by the PFC OVP can be calculated with the equation:

$$Vo_{PFC\_PEAK} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot Vo_{PFC\_NOMINAL} = \frac{2.63V}{2.5V} \cdot Vo_{PFC\_NOMINAL}$$

4.4.2 VOSENSE open loop and short pin detection

The VOSENSE pin, which is sensing the PFC output voltage, has integrated protection circuitry to detect an open and short-circuited pin. This pin can also sense if one of the resistors in the voltage divider is open. Therefore the VOSENSE pin is completely fail-safe. It is not necessary to add an external OVP circuit for the PFC. An internal current source will pull the pin down below the $V_{th(ol)(VOSENSE)}$ detection level of 0.4 V, when the pin is open.Triggering of $V_{th(ol)(VOSENSE)}$ will cause a Safe Restart, see Section 3.4. When the resistor between the VOSENSE pin and ground is open, the OVP will be triggered. In this case, an internal zener clamp will prevent electrical overstress of the VOSENSE pin.

4.4.3 VINSENSE open pin detection

The VINSENSE pin, which senses the mains input voltage, has an integrated protection circuit to detect an open pin. An internal current source will pull the pin down below the $V_{stop(VINSENSE)}$ level of 0.9 V, when the pin is open. In this case, an internal zener clamp will prevent electrical overstress of the VINSENSE pin.

4.4.4 OverCurrent Protection (OCP)

An Over Current Protection (OCP) limits the maximum current through the PFC MOSFET and PFC coil. The current is measured via a current sense resistor in series with the MOSFET source. The MOSFET will be switched of immediately when the voltage at pin PFCSENSE exceeds the $V_{sense(PFC)max}$ level of 0.52 V. The OCP is a switching cycle-by-switching cycle protection.

To avoid false triggering of the PFC OCP by switching of the flyback, it is advised to keep a margin of 0.1 V into account. False triggering of the $V_{OVP(VOSENSE)}$ protection can cause disturbance of the AC mains input current. It is also advised that a small capacitor of 100 pF to 220 pF is placed directly at the PFCSENSE pin to suppress external disturbance.

The current sense resistor can be calculated as follows:

$$R_{OCP(PFC)} = \frac{V_{sense(PFC)max} - V_{margin}}{Ip_{QR(PFC)max}} = \frac{0.52V - 0.1V}{Ip_{QR(PFC)max}}$$

Where: $I_{pQR(PFC)max}$ is the maximum PFC peak current at the high load and low mains.

For the PFC operating in Quasi Resonant mode the maximum peak current can be calculated as follows:

$$Ip_{QR(PFC)max} = \frac{2\sqrt{2} \cdot Pi_{max} \cdot 1.1}{Vac_{min}} = \frac{2\sqrt{2} \cdot \frac{Po_{max}}{\eta} \cdot 1.1}{Vac_{min}}$$

Where:

- Po_{max} is the maximum output power of the flyback
- 1.1 is a factor to compensate for the dead time between zero current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in QR mode
- η is the expected efficiency of the total converter at maximum output power
- Vac_{min} is minimum mains input voltage.

5. Flyback description and calculation

The flyback of the TEA1750 is a variable frequency controller that can operate in Quasi Resonant (QR) or Discontinuous Conduction mode with demagnetization detection and valley switching.

The setting of the primary peak current controls the output power; the switching frequency is a result. The primary peak current is set through the voltage at pin FBCTRL and measured back at the FBSENSE pin with the following relationship:

$$V_{sense(FB)} \cong 0.75 \times V_{FBCTRL} - 1V$$

The flyback controls the operational mode of the PFC. At low output powers, when the primary peak current, $Ip \leq 0.25 \times Ip\_max$, the PFC is set in Burst mode.

Demagnetization of the flyback transformer is detected through the FBAUX pin, connected to the auxilary winding. The valley is detected through pin HV, which can be connected to the MOSFET drain or to the center tap of the primary winding.

The flyback has an accurate Over Voltage Protection (OVP) circuit. The overvoltage is measured, through the FBAUX pin. Both controllers will be switched off in a latched protection when an overvoltage is detected.

5.1 Flyback output power control

An important aspect of the TEA1750 flyback system is, that the setting of the primary peak current controls the output power. The switching frequency is a result of external application parameters and internal IC parameters.

External application parameters are the transformer turns ratio, the primary inductance, the drain source capacitance, the input voltage, the output voltage and the feedback signal from the control loop. Internal IC parameters are the oscillator setting, the setting of the peak current and the detection of demagnetization and valley.

The output power of flyback can be described with the equation:

$$Po = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot fs \cdot \eta$$

At initial start-up, the flyback will always start at the maximum output power. From maximum to minimum output power, the flyback will go through the three operation modes as shown in Figure 12.

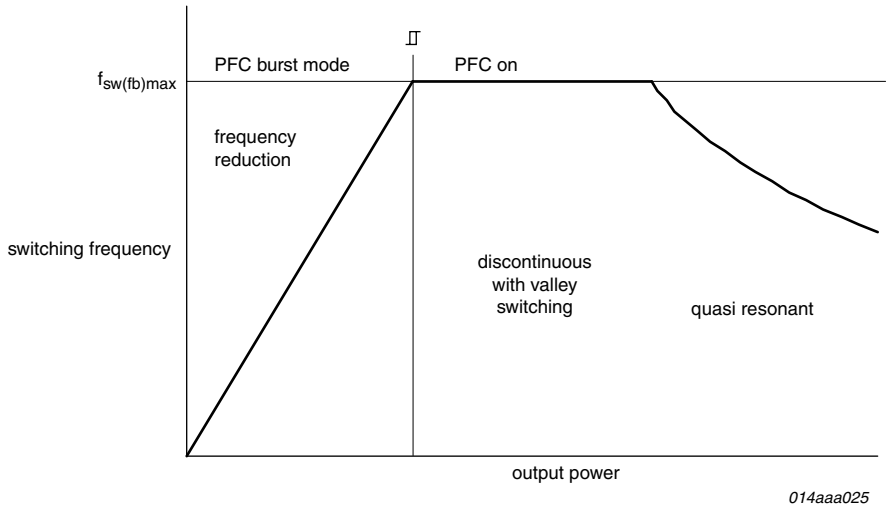

Fig 12. Operation modes flyback

At maximum output power, limited by the flyback current sense resistor, the flyback operates in Quasi Resonant (QR) mode. The next primary switching cycle starts at detection of the first valley.

By reducing the peak current, the output power is reduced and as a result the switching frequency goes up. When the maximum flyback switching frequency is reached and the output power still has to be reduced, the flyback goes from QR into Discontinuous mode (DCM) with valley switching.

In DCM the output power is reduced by further reduction of the peak current and at the same time skipping of one or more valleys. In this mode, the switching frequency is kept constant. The exact switching frequency however, depends on the detection of the valley but will never be higher as the maximum frequency.

The minimum flyback peak current: At this point the flyback enters the Frequency Reduction mode and the PFC is set in Burst mode. In the Frequency Reduction mode the peak current is kept constant. Increasing the off time reduces the output power.

It is advised to place a 10 nF noise filter capacitor C15 (Figure 1) as close as possible to the FBTRL pin to avoid disturbance of the flyback by switching of the PFC MOSFET.

5.1.1 Calculation of the flyback current sense resistor

The current sense resistor $R_{OCP(fb)}$ can be calculated by:

$$R_{OCP(fb)} = \frac{V_{sense(fb)max}}{Ip_{QR(fb)max}} = \frac{0.52V}{Ip_{QR(fb)max}}$$

For the flyback operating in Quasi-resonant mode the peak current can be calculated by:

$$Ip_{QR(fb)max} = \frac{2Po_{max} \cdot 1.1}{\eta \times Vdc_{min}} \times \frac{Vdc_{min} + \frac{Np}{Ns} \cdot Vo}{\frac{Np}{Ns} \cdot Vo}$$

Where:

- Po_{max} is the maximum output power of the flyback
- 1.1 is a factor that compensates for the dead time between zero current in the flyback transformer at the end of the secondary stroke and the detection of the first valley in QR mode;
- η is the expected efficiency of the flyback at maximum output power

  Vdc_{min} is minimum bulk elcap voltage in PFC Burst mode as follows:

$$Vdc_{min} = Vo_{PFC} \times \frac{V_{burst(L)}}{V_{reg(VOSENSE)}} = Vo_{PFC} \times \frac{1.92V}{2.5V}$$

- Vo is the output voltage
- Np is the number of primary turns of the flyback transformer
- Ns is the number of secondary turns of the flyback transformer.

5.1.2 Calculation of the flyback soft start components

The soft start is implemented through the RC network at pin FBSENSE.

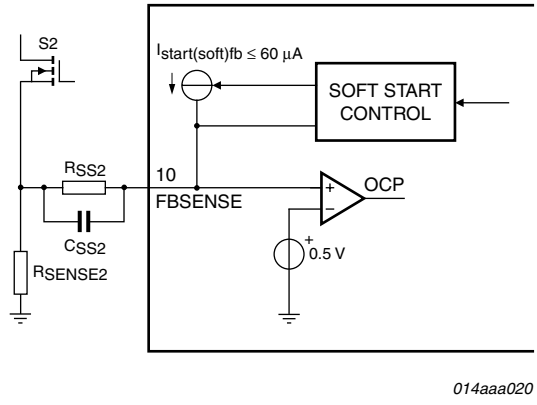

Fig 13. Flyback soft start

Rss2 must have a minimum value of 12 kΩ as specified. This to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable start-up of the flyback. See Section 3.1 for start-up description.

The total soft start or soft stop time is equal to: $t_{softstart} = 3Rss2 \cdot Css2$. It is advisable to make the soft start time for the flyback larger than the soft start time of the PFC, to make sure that the PFC starts before the flyback at initial start-up. It is also advisable to keep the soft start time in a range of 5 ms to 10 ms.

With C10 = 220 nF and R16 = 12 kΩ (see Figure 1) the total soft start time will be 8 ms.

5.2 Flyback control of PFC Burst mode

The flyback controls the Operation mode of the PFC. At low output powers, when the primary peak current $Ip \leq 0.25 \times Ip\_max$, the PFC is set in Burst mode. This is the same point as when the flyback enters the Frequency Reduction mode, see Figure 12 and Section 4.1.

On the transition from PFC Normal mode to Burst mode and from Burst mode to Normal mode is a hysteresis of 60 mV $V_{hys(FBCTRL)}$ on V_{FBCTRL}. This provides the possibility of smooth transitions for all applications. It is advised to place the 10 nF noise filter capacitor C15 (see Figure 1) as close as possible to the FBTRL pin in order to guarantee a smooth transition from PFC burst to PFC Normal mode and to avoid audible noise in flyback transformer.

5.3 Flyback protections

5.3.1 Short circuit on the FBCTRL pin

If the pin is shorted to ground, switching of the flyback controller is blocked. This situation is equal to the minimum, or no output, power situation.

5.3.2 Open FBCTRL pin

As shown in Figure 15. the FBCTRL pin is connected to an internal voltage source of 3.5 V via an internal resistor of 3 kΩ. As soon as the voltage on pin FBCTRL is above 2.5 V, this connection is disabled and the FBCTRL pin is biased with an internal 30 μA current source. When the voltage on the FBCTRL pin rises above $V_{to(FBCTRL)}$ of 4.5 V a fault is assumed. Switching of the flyback (and also the PFC) is blocked and the controller will enter the Safe Restart mode.

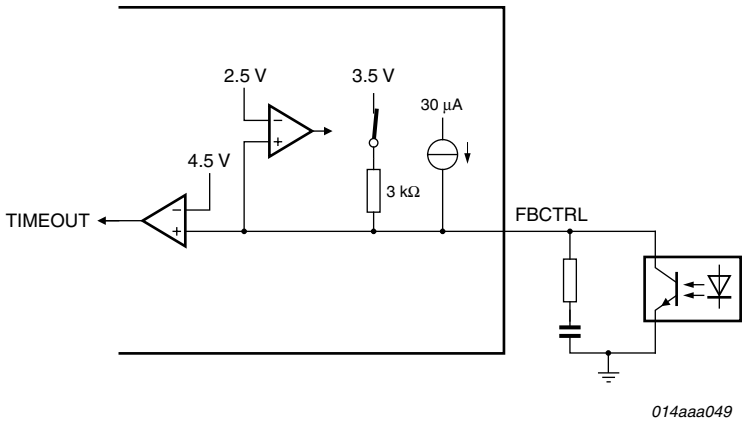

Fig 14. Time-out protection, block diagram

5.3.3 Time-out flyback control-loop

A time-out function can be realized to protect for an output overload short or for an open control loop situation, see Figure 15. This can be done by placing a resistor in series with a capacitor between the FBCTRL pin and ground. See Figure 15. Above 2.5 V the switch in series with the resistor of 3 kΩ is opened and pin FBCTRL and thus the RC combination is biased with a 30 μA current-source. When the voltage on FBCTRL pin rises above 4.5 V, switching of the flyback (and also the PFC) is blocked and the controller will enter the Safe Restart mode. The capacitor is used to set the time to reach 4.5 V at the FBCTRL pin. In Safe Restart mode an internal switch pulls the FBCTRL pin down to discharge the timing capacitor. The resistor is necessary to separate the relative large time-out capacitor from the control loop response. It is advised to use a resistor of at least 30 kΩ. The resistor however, will also influence the charge time of the capacitor.

The time-out time t_{to} can be calculated by:

$$t_{to} = \frac{C_{to} \cdot (V_{to(FBCTRL)} - (I_{0(FBCTRL)} \cdot R_{to}))}{I_{O(FBCTRL)}}$$

otherwise the capacitor can be calculated by:

$$C_{to} = \frac{I_{O(FBCTRL)} \cdot t_{to}}{V_{to(FBCTRL)} - (I_{O(FBCTRL)} \cdot R_{to})}$$

or the resistor can be calculated by:

$$R_{to} = \frac{V_{to(FBCRTL)}}{I_{O(FBCRTL)}} - \frac{t_{to}}{C_{to}}$$

A t_{to} of 37 ms in combination with a C_{to} of 330 nF leads to a resistor value of:

$$R_{to} = \frac{4.5V}{30\mu A} - \frac{37ms}{330nF} = 37.9k\Omega \approx 39k\Omega$$

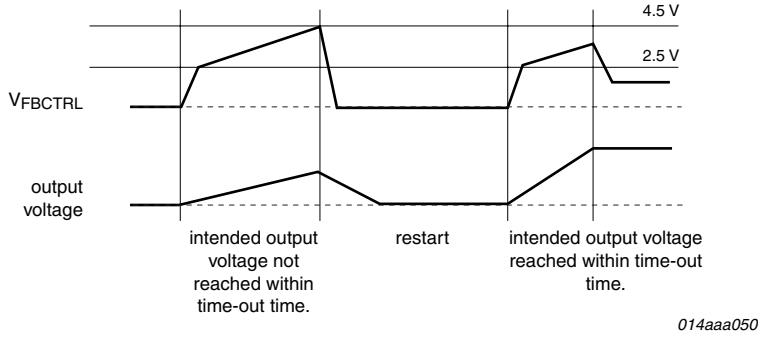

Fig 15. Time-out protection, timing diagram

5.3.4 Overvoltage protection flyback

The IC has an internal Over Voltage Protection (OVP) circuit, which will switch off both controllers when an overvoltage is detected at the output of the flyback, by a latched protection. The IC can detect an overvoltage at a secondary winding of the flyback by measuring the voltage at the auxiliary winding during the secondary stroke. A series resistor between the auxiliary winding and the FBAUX pin converts this voltage to a current on the FBAUX pin.

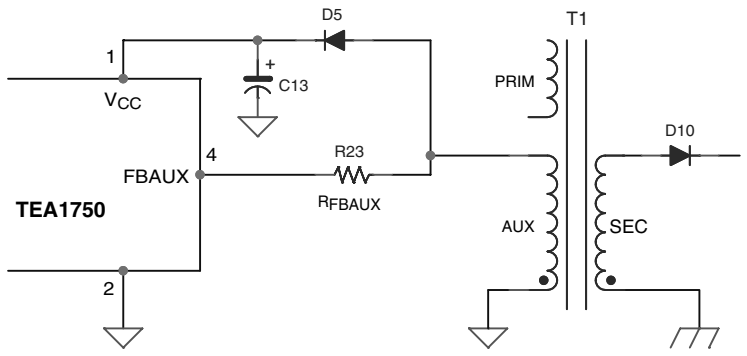

Fig 16. Flyback OVP setting with R_{OVP}

At a current $I_{ovp(FBAUX)}$ of 300 μA into the FBAUX pin, the IC detects an overvoltage. An internal integrator filters noise and voltage spikes. The output of the integrator is used as an input for an up-down counter. The counter has been added as an extra filter to prevent false OVP detection, which might occur during ESD or lightning events.

If the integrator detects an overvoltage then the counter increases its value by one. If another overvoltage is detected during the next switching cycle then the counter increases its value by one again. If no overvoltage is detected during the next switching cycle, then the counter will subtract its value by two (the minimum value is 0). If the value reaches 8, the IC assumes a true overvoltage, and activates the latched protection. Both converters will be switched off immediately and V_{CC} will start cycling between the $V_{TH(UVLO)}$ and $V_{STARTUP}$, without a restart.

Switching off and then switching on the mains input voltage, will trigger the fast latch reset circuit, and reset the latch.

The OVP level can be set by the resistor R_{OVP}:

$$R_{OVP} = \frac{\left(\frac{N_{AUX}}{N_S} \times Vo_{OVP}\right) - V_{clamp(FBAUX)}}{I_{OVP(FBAUX)}} = \frac{\left(\frac{N_{AUX}}{N_S} \times Vo_{OVP}\right) - 0.7V_{(typ)}}{300\mu A_{(typ)}}$$

Where:

- N_S is the number of turns on the secondary winding
- N_{aux} is the number of turns on the auxiliary winding of the flyback transformer
- $V_{clamp(FBAUX)}$ is the positive clamp-voltage of the FBAUX pin.

For the calculation of the Vo_{OVP} level the tolerances on $I_{ovp(FBAUX)}$ have to be taken into account, this to avoid triggering of the OVP during normal operation.

6. References

[1] **IEC-60950 —** Chapter 2.1.1.7 “discharge of capacitors in equipment”

[2] IEC61000-3-2 **—**

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